Customer No. 22,852
Attorney Docket No. 02887.0269

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Katsuhiko HIEDA et al.	)	
	)	Group Art Unit: Not assigned
Application No.: Not Yet Assigned	)	
	)	Examiner: Not assigned
Filed: March 19, 2004	)	
	)	
For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Except for the U.S. patent and patent publication, copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

The following is a concise statement of relevance of the non-English language documents:

1. Japanese Patent Application No. P2000-114362 discloses an STI structure with SOG film and HTO film. (Fig.3 and lines 14-17 of left portion of page 3).

The relevance of this document is also discussed at page 6 of the specification of the present application. An English language abstract of this document is enclosed.

2. Japanese Patent Application No. P2000-183150 discloses an STI structure with SOG (lower portion) and HDP-SiO_2 CVD (upper portion). (Fig. 3). The relevance of this document is also discussed at page 6 of the specification of the present application. An English language abstract of this document is enclosed.

3. Japanese Patent Application No. 2001-308090 discloses SOG film to fill STI, which has a solution including polysilazane, having a weight average molecular weight within the range of about 3,000 - 20,000. (Fig 3). The relevance of this document is discussed at page 6 of the specification of the present application. An English abstract of this document is enclosed.

4. Japanese Patent Application No. 2002-203895 discloses an STI Structure with an Si_3N_4 liner and SOG film and CVD-SiO_2 film (Fig. 10).

An English abstract of this document is enclosed.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the Office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed

documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: March 19, 2004

By: _____
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Enclosures
RVB/FPD/dvg

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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	02887.0269	Application No.	
Applicant	Katsuhiko HIEDA et al.		
Filing Date	March 19, 2004	Group:	Not assigned

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,479,405 B2	11/12/02	Lee et al.			
		2003/0022522 A1	1/30/03	Nishiyama et al.			

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2000-114362	4/21/00	Japan			Abstract
		2000-183150	6/30/00	Japan			Abstract
		2001-308090	11/2/01	Japan			Abstract
		2002-203895	7/19/02	Japan			Abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Jin-Hwa Heo et al., "Void Free and Low Stree Shallow Trench Isolation Technology using P-SOG for sub 0.1 μm Device". Symposium On VLSI Technology Digest of Technical Papers. pp. 132-133 (2002)
	Yukio NISHIYAMA et al., "Method for Manufacturing Semiconductor Device", U.S.Serial No. 10/193,143, filed July 12, 2002.

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce